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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,699	12/18/2001	Chi-Keung Luk	1662-46800 JMH (P01-3627)	3236

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EXAMINER	
NGO, KIET TUAN	

ART UNIT	PAPER NUMBER
2195	

DATE MAILED: 06/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,699	LUK ET AL.	
	Examiner	Art Unit	
	Kiet T. Ngo	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/09/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 36 are pending in this application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1 – 30 and 33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. The following claim language is indefinite:

(i) As to claims 1, lines 8 – 9; claim 10, lines 8 – 9; and claim 19, lines 5 – 6; it is unclear as to how a main program can be running and spawn a pre-execution thread and have that pre-execution thread run ahead of that currently running program (i.e. how is the main program which was running first ever be running behind a program which was created after the main program?).

(ii) As to claims 5, lines 1 –2, and claim 15, lines 1 - 2, it is uncertain as to how the processor "determines whether sufficient hardware resources" are available (i.e. upon what criteria does the processor make this determination as to whether or not to spawn a process?);

(iii) As to claim 33, lines 1 – 2, it is unclear as to how a pre-execution thread "spins" on a variable (i.e. what does the pre-execution thread do in order to "spin" a predetermined value in relationship to threads to pre-execute?);

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1 – 36 are rejected under 35 U.S.C. 102(a) as being unpatentable over Rotenberg (AR-SMT: A Microarchitectural Approach to Fault Tolerance in Microprocessors).

6. As to claim 1, Rotenberg teaches the invention substantially as claimed, including a computer system [Fig. 1], comprising:

a processor capable of executing multiple threads [Processor, Fig. 1(b); Abstract pg. 1, Left column, line 18];

a I/O controller coupled to said processor [pg. 3, Right column, line 2];

an I/O device couple to said I/O controller [pg. 4, Left column, lines 30 – 33; pg. 5, Right column, lines 1 - 7];

a main system memory coupled to said processor [Memory where program p is stored, Fig. 1(b); pg. 2, Right column, line 52];

wherein said processor processes a program in a main thread that includes instructions [Fig. 1(b); instr i, pg. 2, Right column, lines 45 – 46];

which cause the processor to spawn a preexecution thread in which at least at least a portion of the same program executes [Fig. 1(b); instr i, spawn i + i'], said pre-execution thread runs concurrently with the main thread (pg. 2, Left column, lines 28 – 29; Fig. 1(b), parallel execution units], but ahead of the main thread in program order [Fig. 3, pg. 3, Right column, lines 7 - 10].

7. As to claim 10, 31, and 32, they are rejected for the same reason as claim 1 above, in addition Rotenberg further teaches the processor comprising:

a fetch unit capable of fetching instructions from a plurality of threads [pg. 3, Right column, line 2];

a program counter coupled to said fetch unit [pg. 5, Right column, lines 15 - 16];

an instruction cache coupled to said fetch unit [Fig. 5, Trace Cache];

a data cache coupled to said instruction cache [Fig. 5, Fetch, Dispatch, issue execute (D-Cache)];

8. As to claim 19, Rotenberg teaches the invention as claimed in claim 1 and 10, in addition, Rotenberg teaches of inserting instructions to generate a pre-execution thread in a processor into a program:

(a) inserting pre-execution thread instructions in the program [Fig. 1(b); Fig. 3(a); Branch inst];

(b) spawning a pre-execution thread when designated by the inserted instruction [Fig. 1(b) instr i']; and running said pre-execution thread concurrently with a main thread

wherein both the pre-execution and the main threads include instructions from the same program, the pre-execution thread running ahead of the main thread [Fig. 1(b); pg. 2, Left column, lines 28 – 29; Fig. 3; pg. 3, Right column, lines 7 – 10;

9. As to claim 2, 11, 20, 28, and 30, Rotenberg teaches of a start instruction (branch - start), which causes the pre-execution thread to start, and a stop instruction (branch - return), which causes the pre-execution thread to stop. [Fig. 3(a)]

10. As to claims 3, 12, and 29, Rotenberg discloses starting an instruction at a value in the program (i.e. branch address) [Fig. 3(a)].

11. As to claims 4, and 13, Rotenberg wherein the pre-execution thread encounters a cache miss condition for a memory reference but the main thread does not encounter a cache miss condition when that same memory reference is processed by the main thread [pg. 5, Right column, lines 1 – 14].

12. As to claims 5, 14, and 22, Rotenberg discloses his processor scavenging idle execution cycles before executing the redundant computations [pg. 2, Left column, lines 28 - 31]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have recognized this scavenging as determining whether resources are available to spawn the pre-execution thread.

13. As to claims 6, 15, and 23, Rotenberg teaches ignoring exception conditions generated during pre-execution thread. [pg. 6, Right column, lines 22 - 27].

14. As to claims 7, 8, 16, 17, 24, and 27, Rotenberg teaches storing the results of the initial program running onto a FIFO queue called the Delay Buffer which includes modifications to registers and memory, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have recognized that by storing the results into a buffer it doesn't allow a store instruction to occur within any of the initial running of the program. [pg. 2, Left column, lines 45 - 52]

15. As to claims 9, 18, and 26, Rotenberg teaches of a buffer, which stores results of each instruction. [pg. 2, Right column, lines 45 - 52]

16. As to claim 21, Rotenberg teaches copying register contents with the main thread to registers used by the pre-execution thread [pg. 5, Left column, lines 34 - 37].

17. As to claim 25, Rotenberg discloses copy the contents of at least one register to memory to make such register contents available to pre-execution threads [pg. 5, Left column, lines 34 - 37].

18. As to claim 33, Rotenberg discloses starting an instruction at a value in the program (i.e. branch address) [Fig. 3(a)].

19. As to claim 34, Rotenberg discloses of stopping instructions when a program counter exceeds a range [pg. 6, Left column, lines 34 – 38].

20. As to clam 35, Rotenberg teaches the stopping the pre-executing instructions when the main thread catches up with the pre-executing instructions [pg. 6, Left column, lines 24 - 26].

21. As to claim 36, Rotenberg teaches of stopping the pre-execution instructions when the number of pre-executing instructions exceeds a limit [pg. 6, Left column, lines 23 - 24].

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
Vosbury (U.S. Patent #5,138,708), discloses CPUs executing the same instruction set.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiet T. Ngo whose telephone number is (571)272-6451. The examiner can normally be reached on Mon. - Fri. 830-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-An Ai can be reached on (571)272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KTN

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